

What is claimed is:

- 1        1.        A method of forming a crystalline polysilicon gate electrode structure on a gate  
2        dielectric, comprising the steps of:  
3                depositing on the gate dielectric polysilicon crystals of substantially a first size; and  
4                contiguously with the crystals of the first size depositing directly thereon additional  
5        polysilicon crystals of substantially a second size.
- 1        2.        The method according to claim 1, wherein:  
2                the first crystal size is larger than the second crystal size.
- 1        3.        The method according to claim 1, wherein:  
2                the first crystal size is smaller than the second crystal size.
- 1        4.        A method of forming a crystalline polysilicon gate electrode structure on a gate  
2        dielectric, comprising the step of:  
3                controlling a variation of at least one of temperature, pressure, and flow rate of a  
4        continuous flow of silane or related silicon precursor species while depositing polysilicon  
5        therefrom as crystals of correspondingly controlled grain size.
- 1        5.        The method according to claim 4, wherein:  
2                the variation is controlled in step-wise manner, to thereby form a multi-region  
3        polycrystalline silicon deposit comprising regions having crystals of respective grain sizes.
- 1        6.        The method according to claim 5, wherein:  
2                crystals deposited in a first region adjacent to the gate dielectric have a first grain  
3        size selected to maximize dopant activation near the gate dielectric and a second region that  
4        has crystals of a second grain size deposited more distantly from the gate dielectric.
- 1        7.        A method of forming a polycrystalline silicon structure in which crystal grain size  
2        varies as a function of depth, comprising the step of:

3           controlling a variation of at least one of temperature, pressure, and flow rate of a  
4           silane gas while depositing silicon therefrom, to thereby control the crystal grain size as a  
5           function of depth in the deposited polysilicon structure.

6           8.       The method according to claim 7, wherein:  
7                   the polysilicon structure comprises a plurality of regions having respective grain  
8                   sizes.

1           9.       The method according to claim 8, wherein:  
2                   the polycrystalline silicon structure is a gate electrode formed on a gate dielectric,  
3                   and comprises a first region having a first crystal grain size and a second region formed  
4                   thereon and having a second grain size,  
5                   wherein the first and second grain sizes are selected to maximize dopant activation  
6                   in the first region and to achieve a specific resistance in the second region.

1           10.      The method according to claim 9, further comprising:  
2                   a third region formed on the second region and having crystals of a third grain size,  
3                   to further tailor the resistance of the gate conductor structure.

1           11.      The method according to claim 8, wherein:  
2                   the electrical resistance of the deposited silicon varies inversely with the controlled  
3                   pressure.

1           12.      The method according to claim 7, comprising the further step of:  
2                   providing a controlled flow of a dopant gas during a selected portion of the step of  
3                   depositing polysilicon, to thereby enable selected doping or counter-doping of a portion of  
4                   the deposited polysilicon.

1           13.      The method according to claim 12, wherein:  
2                   the dopant gas is selected to provide one of a p-type or an n-type doping during a  
3                   final portion of the step of depositing polysilicon.

- 1 14. The method according to claim 7, comprising the further step of:  
2 forming a layer rich in carbon atoms at a selected stage of the silicon deposition.
- 1 15. The method according to claim 7, comprising the further step of:  
2 forming a layer of silicon-germanium at a selected stage of the silicon deposition.
- 1 16. The method according to claim 7, wherein:  
2 the variation is controlled to deposit the polysilicon so that the crystal grain size  
3 varies monotonically during the deposition of the polysilicon.
- 1 17. A CMOS transistor comprising a gate conductor formed on a gate dielectric,  
2 wherein the gate conductor comprises a multi-region polycrystalline silicon, comprising:  
3 a first region adjacent the dielectric and comprising silicon crystals of a first grain  
4 size; and  
5 a second region formed contiguously with and over the first region and comprising  
6 silicon crystals of a second grain size.
- 1 18. The CMOS transistor according to claim 17, wherein:  
2 the first and second grain sizes are selected to maximize a dopant activation near the  
3 gate dielectric in the first region and to achieve a specific resistance in the second region.
- 1 19. The CMOS transistor according to claim 18, wherein:  
2 an upper portion of the polysilicon structure is consumed by silicide.
- 1 20. The CMOS transistor according to claim 18, further comprising:  
2 a third region formed contiguously with and over the second region, the third region  
3 serving to further tailor the resistance of the gate conductor.
- 1 21. A doped polysilicon resistor structure, comprising:  
2 an insulator; and

3           a multi-region polycrystalline silicon conductor structure, comprising regions having  
4           silicon crystals of respectively different sizes, formed over the insulator.

1       22.    The structure according to claim 20, wherein:  
2           the silicide formation is blocked by a layer of nitride.